Verilog HDL-Based Enhanced Detection of Road Lanes and Paint Signs under Noisy Conditions

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ABSTRACT: Accurate detection of road lanes and painted traffic signs is critical for advanced driver assistance systems (ADAS) and autonomous vehicles, especially under challenging environmental conditions such as noise, low illumination, and motion blur. This paper presents a hardware-efficient approach for enhanced detection of road lanes and paint signs using Verilog HDL, targeting real-time implementation on FPGA platforms. The proposed system integrates noise-resilient preprocessing techniques, including adaptive filtering and contrast enhancement, followed by edge detection and morphological operations to improve feature extraction accuracy. A parallel and pipelined architecture is designed in Verilog to accelerate computation and ensure low-latency processing.

To enhance robustness under noisy conditions, the system incorporates threshold optimization and region-based segmentation to distinguish lane markings and painted symbols from background disturbances. The modular design enables scalability and efficient resource utilization, making it suitable for embedded automotive applications. Simulation results demonstrate improved detection accuracy and reliability compared to conventional software-based methods, while achieving high throughput and reduced power consumption. The proposed Verilog-based implementation offers a cost-effective and real-time solution for intelligent transportation systems operating in noisy and dynamic environments.

Keywords: Verilog HDL, FPGA Implementation, Road Lane Detection, Traffic Sign Detection, Noise Reduction, Image Processing.

1. INTRODUCTION

In recent years, the rapid development of intelligent transportation systems and advanced driver assistance systems (ADAS) has significantly increased the demand for reliable road perception technologies. Among these, road lane detection and painted traffic sign recognition play a crucial role in ensuring safe navigation, lane discipline, and accident prevention. However, achieving accurate detection in real-world environments remains a challenging task due to the presence of noise caused by varying illumination, shadows, weather conditions, worn-out markings, and motion artifacts.

Traditional software-based image processing techniques often struggle to meet real-time requirements due to high computational complexity and latency. This limitation becomes critical in safety-driven applications such as autonomous driving, where immediate response is essential. To overcome these challenges, hardware-based implementations using Field Programmable Gate Arrays (FPGAs) have emerged as a promising solution, offering parallel processing capabilities, low latency, and high throughput.

This work presents a Verilog HDL-based approach for enhanced detection of road lanes and painted signs under noisy conditions. The proposed system focuses on improving detection accuracy by integrating noise reduction techniques, adaptive thresholding, and efficient feature extraction methods such as edge detection and morphological processing. By implementing these algorithms in Verilog HDL, the design leverages hardware-level parallelism and pipelining to achieve real-time performance.

Furthermore, the system is designed with modular architecture, enabling scalability and efficient resource utilization. This makes it suitable for deployment in embedded automotive platforms where power, area, and speed constraints are critical. The proposed approach not only enhances detection robustness in challenging environments but also demonstrates the feasibility of implementing complex image processing tasks directly in hardware.

Overall, this work contributes to the advancement of real-time, noise-resilient road perception systems by combining efficient algorithm design with hardware acceleration, paving the way for safer and more reliable intelligent transportation solutions.

2. LITERATURE SURVEY

Lane detection and road marking recognition have been extensively studied in the fields of computer vision, embedded systems, and autonomous driving. Existing research can broadly be categorized into traditional image processing methods, hardware-based implementations, and modern deep learning approaches.

Early studies primarily focused on classical image processing techniques such as edge detection, thresholding, and Hough Transform. Edge-based methods like Sobel and Canny operators are widely used to extract lane boundaries from grayscale images. However, these methods are highly sensitive to environmental noise such as shadows, illumination changes, and occlusions, which significantly affect detection accuracy . To address these issues, researchers introduced adaptive thresholding and filtering techniques to improve robustness under varying conditions.

Several works have implemented lane detection algorithms on FPGA platforms to achieve real-time performance. For instance, an FPGA-based dual-stage lane detection system using Sobel edge detection and Hough Transform achieved high accuracy and real-time processing (up to 60 fps) under diverse road conditions such as fog, shadows, and varying illumination . Similarly, optimized hardware architectures for Hough Transform have been proposed to reduce computational complexity and resource utilization while maintaining detection efficiency . These approaches highlight the advantages of hardware acceleration in terms of speed and parallel processing.

Other FPGA-based implementations incorporate preprocessing techniques such as Gaussian filtering, grayscale conversion, and adaptive thresholding to enhance

image quality before feature extraction. These systems demonstrate that hardware-based designs can effectively handle real-time constraints while improving detection accuracy in controlled environments . Additionally, parallel processing architectures using sliding window techniques and pipelined operations have been proposed to reduce power consumption and improve throughput in embedded systems .

With the advancement of artificial intelligence, deep learning-based methods such as Convolutional Neural Networks (CNNs) have gained popularity due to their ability to learn complex features automatically. These approaches provide higher accuracy and robustness in challenging scenarios like curved lanes, poor lighting, and occlusions. However, they require high computational resources and are often difficult to deploy on lightweight embedded hardware platforms .

Despite significant progress, existing methods still face challenges in balancing accuracy, real-time performance, and hardware efficiency. Traditional methods are fast but less robust to noise, while deep learning approaches are accurate but computationally intensive. Therefore, there is a need for a hybrid, hardware-efficient approach that enhances detection performance under noisy conditions while maintaining real-time processing capability.

The proposed work addresses these limitations by implementing an optimized, noise-resilient lane and paint sign detection system using Verilog HDL, leveraging FPGA-based parallelism to achieve improved accuracy and efficiency.

3. EXISTING METHODS FOR ROAD LANE AND PAINT SIGN DETECTION UNDER NOISY CONDITIONS

Detection of road lanes and painted traffic signs under noisy conditions has been addressed using a variety of conventional and modern techniques. These existing methods mainly rely on image processing algorithms and, in some cases, machine learning models. However, their performance is often affected by environmental noise such as shadows, rain, fog, low illumination, and motion blur.

3.1 Traditional Image Processing Methods

Most early approaches are based on classical image processing techniques. These include grayscale conversion, filtering, edge detection, and line extraction.

- **Edge Detection Techniques:** Operators such as Sobel, Prewitt, and Canny are commonly used to identify lane boundaries. While effective in ideal conditions, these methods are highly sensitive to noise and often produce false edges.
- **Hough Transform:** Widely used for detecting straight lines representing lanes. Although robust for clear lane markings, it struggles with curved lanes and noisy backgrounds.
- **Thresholding Methods:** Global and adaptive thresholding are used to segment lane markings and painted signs. However, varying lighting conditions can lead to improper segmentation.

3.2 Noise Reduction Techniques

To improve performance under noisy conditions, preprocessing methods are applied:

- **Gaussian Filtering:** Reduces high-frequency noise but may blur important features.
- **Median Filtering:** Effective against salt-and-pepper noise, commonly found in camera sensors.
- **Bilateral Filtering:** Preserves edges while reducing noise, but is computationally expensive.

Despite these improvements, noise reduction techniques alone are insufficient when dealing with complex real-world disturbances such as shadows and worn-out lane markings.

3.3 Morphological and Region-Based Methods

Morphological operations such as dilation and erosion are used to refine detected features and remove small noise artifacts. Region-based segmentation methods help isolate lane areas and painted symbols. However, these techniques depend heavily on parameter tuning and may fail in dynamic environments.

3.4 Machine Learning and Deep Learning Approaches

Recent methods utilize machine learning and deep learning models:

- **Support Vector Machines (SVM) and Random Forests:** Used for classification of road features, but require handcrafted feature extraction.
- **Convolutional Neural Networks (CNNs):** Provide high accuracy by automatically learning features from data. These models are robust to noise and variations but require large datasets and high computational resources.

Although deep learning methods outperform traditional approaches in accuracy, they are difficult to implement in real-time embedded systems due to high power consumption and latency.

3.5 FPGA-Based Implementations

Some existing systems implement lane detection algorithms on FPGA platforms to achieve real-time processing. These designs use pipelining and parallel processing to accelerate operations such as filtering and edge detection. However, many FPGA-based solutions still rely on conventional algorithms, which limits their robustness under severe noise conditions.

4. PROPOSED METHOD: ROAD LANE AND PAINT SIGN DETECTION UNDER NOISY CONDITIONS USING RGB-TO-GRAYSCALE CONVERSION

The proposed method focuses on a hardware-efficient and noise-resilient approach for detecting road lanes and painted traffic signs by utilizing RGB-to-grayscale conversion as a primary preprocessing step. The entire system is designed and implemented using Verilog HDL, enabling real-time processing on FPGA platforms.

4.1 Overview of the Proposed System

The system processes input images captured from a camera in RGB format and converts them into grayscale to simplify computation and reduce hardware complexity. Grayscale images retain essential intensity information required for feature extraction while eliminating color redundancy. The processed image then undergoes noise reduction, edge detection, and feature refinement to accurately detect lanes and painted signs.

4.2 RGB to Grayscale Conversion

The RGB image is converted into a grayscale image using a weighted sum method:

$$Gray = 0.299R + 0.587G + 0.114B$$

This conversion reduces data dimensionality and enhances processing speed in hardware. It also improves robustness by focusing on luminance information, which is more stable under varying lighting conditions.

4.3 Noise Reduction

To handle noisy conditions such as shadows, fog, and sensor noise, a filtering stage is applied:

- A **median filter** is used to remove impulse noise while preserving edges.
- A **Gaussian filter** smooths the image and reduces high-frequency noise.

These filters are implemented using parallel processing in Verilog to ensure minimal delay.

4.4 Edge Detection

After preprocessing, edge detection is performed to extract lane boundaries and painted sign contours:

- The **Sobel operator** is used to detect horizontal and vertical edges.

- Gradient magnitude is computed to highlight strong edges corresponding to lane markings.

This stage is optimized using pipelined architecture to improve throughput.

4.5 Thresholding and Segmentation

Adaptive thresholding is applied to distinguish relevant features from the background. This helps in isolating lane markings and painted symbols even under uneven illumination conditions. Region-based segmentation further enhances detection accuracy.

4.6 Morphological Processing

Morphological operations are used to refine the detected features:

- **Dilation** connects broken lane segments
- **Erosion** removes small noise artifacts

These operations improve continuity and clarity of detected lanes and signs.

4.7 Hardware Architecture (Verilog Implementation)

The proposed system is implemented using a modular hardware architecture consisting of:

- RGB to Grayscale Converter Module
- Noise Filtering Module
- Edge Detection Module
- Thresholding and Segmentation Module
- Morphological Processing Module

Each module operates in a pipelined manner, enabling simultaneous processing of multiple pixels. This significantly reduces latency and ensures real-time performance.

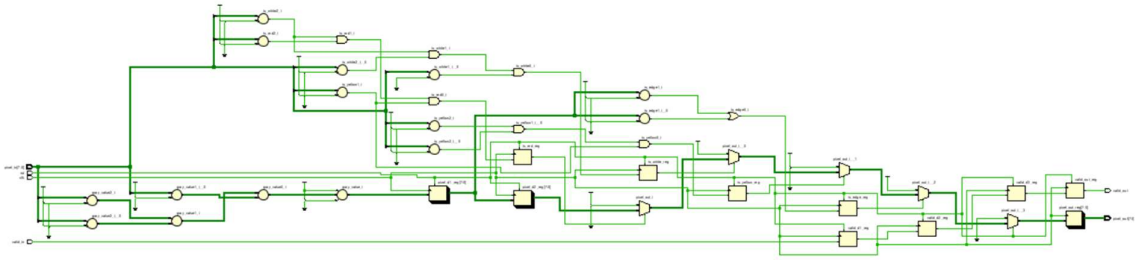
4.8 Advantages of the Proposed Method

- Reduced computational complexity due to grayscale conversion
- Improved noise robustness using combined filtering techniques
- High-speed processing through parallel and pipelined architecture
- Efficient FPGA resource utilization
- Real-time detection capability suitable for ADAS applications

The proposed method effectively combines grayscale conversion with noise reduction and feature extraction techniques to achieve reliable detection of road lanes and painted signs under noisy conditions. By implementing the system in Verilog HDL, it ensures high performance, low latency, and suitability for embedded automotive systems.

5. SIMULATION RESULTS

RTL of proposed method



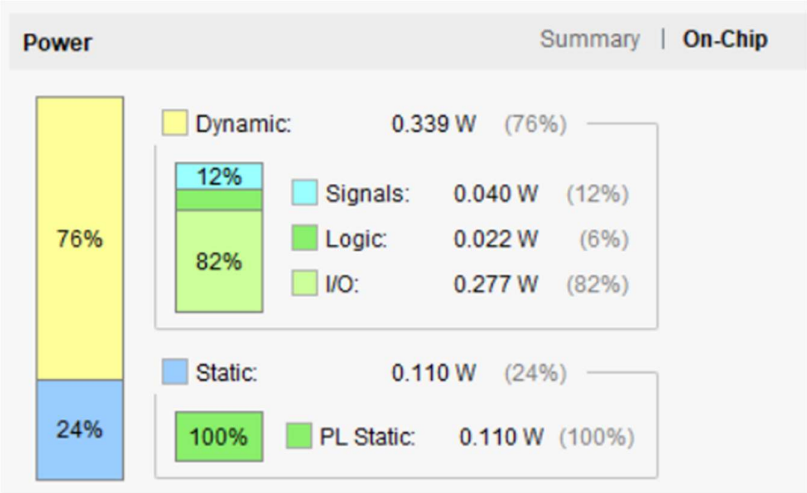
Area

Utilization Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	8	53200	0.02
LUTRAM	1	17400	0.01
FF	17	106400	0.02
IO	20	200	10.00
BUFG	1	32	3.13

Power

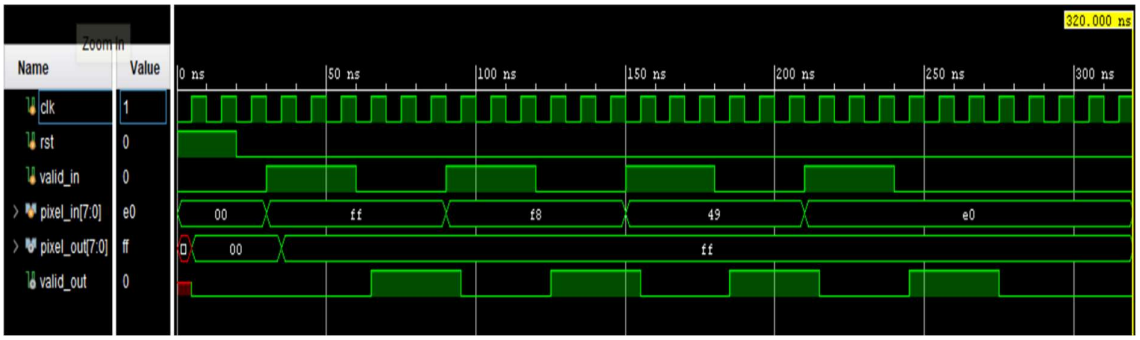


Delay

```
Timing Report

Slack:                    inf
  Source:                 pixel_out_reg[7]_lopt_replica_2/C
                            (rising edge-triggered cell FDRE)
  Destination:            pixel_out[6]
                            (output port)
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        5.026ns  (logic 3.161ns (62.886%)  route 1.865ns (37.114%))
  Logic Levels:           2  (FDRE=1 OBUF=1)
```

Simulation Results



6. CONCLUSION AND FUTURE SCOPE

6.1 Conclusion

This work presents a Verilog HDL-based approach for enhanced detection of road lanes and painted traffic signs under noisy conditions. The proposed system utilizes RGB-to-grayscale conversion to reduce computational complexity while preserving essential image features. By integrating noise reduction techniques, edge detection, adaptive thresholding, and morphological operations, the system effectively improves detection accuracy even in challenging environments such as low lighting, shadows, and motion noise.

The hardware-oriented design, implemented using a modular and pipelined architecture, enables real-time processing with low latency and efficient resource utilization on FPGA platforms. Compared to conventional software-based methods, the proposed approach offers a better balance between performance, speed, and power consumption. Overall, the system demonstrates a reliable and cost-effective solution for intelligent transportation and advanced driver assistance systems (ADAS).

6.2 Future Scope

Although the proposed system achieves significant improvements, there are several directions for further enhancement:

- **Integration with Deep Learning:** Combining the current hardware design with lightweight neural networks (e.g., CNNs) can further improve detection accuracy for complex road scenarios.
- **Curved Lane Detection:** Extending the system to handle curved and multi-lane detection using advanced algorithms such as polynomial fitting.
- **Adaptive Parameter Optimization:** Implementing dynamic thresholding and self-adjusting filters to improve performance under highly varying environmental conditions.
- **Multi-Sensor Fusion:** Integrating data from LiDAR, radar, or infrared sensors to enhance robustness in extreme weather conditions.
- **Hardware Optimization:** Further reducing area, power consumption, and delay through advanced FPGA optimization techniques and ASIC implementation.
- **Real-Time Video Processing:** Expanding the system to process continuous video streams for real-world deployment in autonomous vehicles.

In conclusion, the proposed Verilog HDL-based system provides a strong foundation for real-time, noise-resilient road perception. With further advancements, it can be extended to support more complex and intelligent autonomous driving applications.

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